REMARKS

Claims 1-44 are pending. Claims 1-7, 11, 12, 14-22, 26, and 37-40 including independent claims 1 and 16 were rejected under 35 U.S.C. 102(e) as being anticipated by Dick (6,600,788). Dependent claims 8-10, and 23-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dick in view of Shung ("An integrated CAD System for Algorithm-Specific IC Design", IEEE Transactions on Computer Aided Design, Vol. 10, No. 4, April 1991). Claims 13, 27-29, and 41-44 including independent claim 41 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dick in view of Shung and further in view of Saramaki ("Design of Computationally Efficient Interpolated FIR Filters, IEEE Transactions on Circuits and Systems, Vol. 35, No. 1, January 1998).

The Examiner rejected claims 1-44 under 35 U.S.C. 112(1) as not meeting the enablement requirement, since the specification refers broadly to terms such as multi-rate FIR filter, serial filter, parallel filter, decimating FIR filter, etc. The Applicants respectfully disagree. The terms referred to in the specification such as multi-rate FIR filter, serial filter, parallel filter, decimating FIR filter, etc. are widely used and understood by those of skill in the art. For example, many of the terms are described in textbooks and filter design resources on the Internet. Some examples of textbooks and filter design resources that provide information on the terms known to those of skill in the art include Multirate Digital Signal Processing (ISBN: 0471492043), the Electrical Engineering Handbook (ISBN: 0849385741), the Matlab™ filter design function reference available from www.mathworks.com, and the Multirate FAQ, available from www.dspguru.com/info/faqs/multrate/basics.htm. The terms the Examiner noted are believed to be terms widely used and understood by those of skill in the art and the rejection is believed overcome.

The Examiner rejected claims 1 and 16 under 35 U.S.C. 102(e) as being anticipated by Dick. Dick describes a "FIR filter 13 which receives a sequence of re-quantized input data samples x(n) at an input terminal 22 and produces a sequence of output data samples y(n) at an output terminal 23" (column 3, lines 31-34; "3:31-34"). "Filter coefficients a.sub.0 to a.sub.3 are provided to the second input terminals of multipliers 26.sub.0 to 26.sub.3, and are multiplied by the input data samples at taps 24.sub.0 to 24.sub.3 respectively" (3:42-45). "Once the design of the narrow band filter has been finalized, an FPGA can be programmed to implement that design in a known manner" (5:64-66).

Claims 1 and 16 explicitly recite a filter compiler comprising "a filter resource estimator coupled to the filter spectral response simulator for estimating an implementation cost of the filter." Dick does not teach or suggest a filter compiler including a "filter resource estimator" nor does it teach or suggest a "filter resource estimator coupled to the filter spectral response simulator." The Examiner argues that Dick describes a filter spectral response simulator (4:8-12). The material cited by the Examiner only notes that the FIR filter "can be configured to provide a variety of transfer functions, including low pass, high pass, and bandpass. As known by those skilled in the art, the desired transfer function is determined by selection of filter coefficients a.sub.0 and a.sub.N-1."

No "resource estimator is coupled to the filter spectral response simulator." The Examiner argues that Dick describes a filter resource estimator. However, the material cited by the Examiner only notes that "In a prior art implementation ... the total cost of a direct implementation of a FIR filter is 7672 CLBs... In contrast, in the present invention, ... the CLB count is 3002. Thus, the present invention consumes only 39% of the logic resources of a prior art direct implementation" (7:51-57). The material cited by the Examiner does not teach or suggest a filter resource estimator and mentions only a resource calculation. Dick makes no mention of having "filter resource estimator" "coupled to the filter spectral response simulator for estimating an implementation cost of the filter" as recited in the claims. Consequently, the rejection to independent claims 1 and 16 is believed overcome.

The Examiner rejected claim 41 under 35 U.S.C. 103(a) as being unpatentable over Dick in view of Samaraki. The Examiner acknowledges that Dick does not expressly teach "applying a first clock rule when an input data width is less than or equal to an interpolation factor; and applying a second clock rule when an input data width is greater than the interpolation factor" as recited in claim 41. The Examiner argues that Samaraki teaches this recitation. However, the Examiner does not indicate where Samaraki teaches or suggests "an input data width" and applying a first or a second clock rule if the input data width is less than or equal to or greater than an interpolation factor. Samaraki makes no mention of data widths. In fact, the equation the Examiner cites does not even include data width as a possible variable. Consequently, the rejection to independent claim 41 is believed overcome.

In light of the above remarks relating to independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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